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AGHDAM, FRESHTEH N	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/724,151	JEONG ET AL.	
	Examiner	Art Unit	
	Freshteh N. Aghdam	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 21 November 2007.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-8,10,12,14,16 and 18 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-8,10,12,14,16 and 18 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments filed 1Novembr 21, 2007 have been fully considered but they are not persuasive.

Applicant's Arguments:

Regarding independent claim 1, page 10, argues that the claimed invention is not taught or suggested by Walley "a voltage detector detects control voltage from the control signal of the voltage controlled oscillator."

Regarding independent claims 8, 10, 12, 14, and 16, page 12, the applicant argues that the claimed invention is not taught or suggested by Owen "detecting control voltage of the control signal."

Examiner's Response:

Regarding the first argument set forth above, the examiner disagrees with the applicant because Walley discloses a voltage detector (means 325) being configured to detect control voltage (outputted by means 327) from the control signal of the voltage control oscillator (means 311).

Regarding the second argument set forth above, the examiner disagrees with the applicant because the control voltage signal outputted by the loop filter is inherently detected by the VCO because VCO is an oscillator whose frequency can be changed in response to detected control voltage of the control signal outputted from the loop filter.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Walley (US 6,114,888).

As to claim 1, Walley discloses a phase locked loop frequency synthesizer (Fig. 3) comprising: a phase comparator being configured to compare phases of first and second signals applied thereto with each other and to output outputting a phase error signal when there is a phase difference between the first and second signals (block 305); a loop filter being configured to filter the phase error signal outputted from the phase comparator, to stabilize the filtered phase error signal, and to output a control signal (block 309); a voltage controlled oscillator being configured to control for controlling frequency gain of a signal outputted in response to the control signal outputted from the loop filter (block 317); a divider being configured to divide the frequency of the outputted signal of the voltage controlled oscillator according to a division rate to apply the outputted signal to the phase comparator as the second signal (block 321); a voltage detector (block 325) being configured to detect control voltage (block 327) from the control signal (block 311) inputted to the voltage controlled oscillator (block 325); and a controller being configured to calculate for calculating a variation in gain characteristics of the voltage controlled oscillator (e.g. the voltage

control signal that is outputted from the loop filter and inputted to the VCO) using the control voltage outputted from the voltage detector, wherein the voltage detector is a part of the controller 325 to adjust gain of the loop filter, and to control gain of a loop composed of the phase comparator, the loop filter, the voltage controlled oscillator and the divider to be uniform (blocks 325 and 327).

As to claim 4, Walley further discloses that the loop filter includes a variable gain amplifier (block 313), and voltage gain of the loop filter is controlled by adjusting a gain value of the variable gain amplifier (325 and 327).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Walley, and further in view of Kang (US 5,999,024).

As to claim 2, Walley discloses all the subject matter claimed in claim 1, except for the division value of the divider is set by the controller. Kang discloses a PLL, wherein the division value is set based on a signal outputted from the controller (Fig. 2, block 50), wherein the controller receives a control signal outputted from the loop filter in order to utilize a narrowband VCO that is easy to manufacture (Fig. 2, blocks 20, 50, and 60; Col. 4, lines 51-56). Therefore, it would have been obvious to one of ordinary

skill in the art to incorporate the frequency division value control as disclosed by Kang into the invention of Walley for the reason stated above.

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Walley, and further in view of Davis et al (US 5,166,641).

As to claim 3, Walley discloses that the phase detector includes a charge pump circuit (block 307). However, Walley is not explicit about the phase gain of the phase comparator is controlled by adjusting a current value of a driving bias current source included in the charge pump. Davis discloses a PLL comprising a phase detector that includes a charge pump, wherein the phase gain of the phase detector is controlled by adjusting a current source included in the charge pump circuit in order to ensure that the operational characteristics of the current generators are in agreement prior to the start of each phase correction thus preventing steady-state phase alignment errors from developing between the reference and recovered signals (Fig. 2, block 68; Col. 3, lines 40-48; Col. 4, lines 5-13). Therefore, it would have been obvious to one of ordinary skill in the art to incorporate adjusting the current source of the charge pump by Davis into the invention of Walley for the reason stated above.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Walley.

As to claim 5, Walley further discloses that the voltage detector could be implemented through combinational digital circuits (e.g. in digital domain). It would have been obvious to one of ordinary skill in the art to employ an analog to digital converter if

the voltage signal inputted to the voltage detector is in analog domain. The use of analog to digital converters are well known in the art because of the ease and efficiency with which digital signals can be manipulated. Therefore, it would have been obvious to one of ordinary skill in the art to employ an analog to digital converter as part of the voltage detector for the reason stated above.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Walley, and further in view of Martin et al (US 5,686,864).

As to claim 6, Walley discloses all the subject matter claimed in claim 1, except for the voltage controlled oscillator includes at least two sub-voltage controlled oscillators, and one of the sub-voltage controlled oscillators is activated according to a control signal provided by a controller in order to control the VCO over a wide tuning range and eliminates the need for a single VCO with a large tuning voltage range (Fig. 1, blocks 110, 118, 114, and 112; Col. 1, lines 29-35; Col. 2, lines 35-54; Col. 3, lines 14-16). Therefore, it would have been obvious to one of ordinary skill in the art to select one out of a plurality of VCOs as taught by Martin and incorporate it into the invention of Walley for the reason stated above.

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Walley, and further in view of Kobayashi et al (US 2002/0005764).

As to claim 7, Walley discloses all the subject matter claimed in claim 1, except for the voltage controlled oscillator includes at least one inductor and one capacitor that

determine a frequency band, and frequency gain of the voltage controlled oscillator is varied by controlling an impedance value of the inductor or capacitor. Kobayashi discloses a PLL circuitry that employs a VCO, wherein the VCO includes at least one inductor and one capacitor that determine a frequency band (Abstract), and frequency gain (e.g. rate of change of Kv or Kvco or gain) of the voltage controlled oscillator (VCO) is varied by controlling an impedance value of the inductor or capacitor (Abstract; Fig. 3; Par. 33). Therefore, it would have been obvious to one of ordinary skill in the art to incorporate the teaching of Koabayashi into the invention of Walley in order to improve the system performance by avoiding undesirable characteristics when two oscillation frequencies are controlled in the PLL (Par. 16).

Claims 8, 10, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Owen et al (US 5,079,522).

As to claims 8 and 12, Owen discloses a PLL circuit comprising: a phase detector (Fig. 3, block 7) for comparing phases of first and second signals applied thereto with each other and outputting a phase error signal when there is a phase difference between the first and second signals; a loop filter (block 9) for filtering the phase error signal outputted from the phase detector, stabilizing the filtered phase error signal, and outputting a control signal; a voltage controlled oscillator (block 1) for controlling frequency gain (e.g. tuning sensitivity) of a signal output in response to the control signal outputted from the loop filter (Col. 1, lines 51-61); and a divider (block 6; Col. 2, lines 35-49) for dividing the frequency of the outputted signal of the voltage

controlled oscillator according to a division rate to apply the outputted signal to the phase detector as the second signal, wherein the frequency gain (e.g. rate of change of Kv or Kvco) is represented as the slope or rate of change of the VCO gain (Fig. 1a; Col. 2, lines 19-22). Owen is not explicit about calculating the frequency gain of the VCO as Fin (NI-N2)/ (V1-V2). One of ordinary skill in the art would recognize that the VCO gain (e.g. Kv or Kvco) is a well know parameter that is related to the output signal of the VCO (fo(t)) divided by the input signal of the VCO (V(t)). Also, the relationship between the reference frequency (e.g. Fin as named by the applicant in this claim) and the output frequency of the VCO is fo = N * Fin. Consequently, one of ordinary skill in the art would recognize that the rate of change or slope of the VCO gain is calculated as (fo1-fo2= F1-F2)/ (V1-V2), wherein indicies 1 and 2 corresponds to the first time that the VCO frequency (fo) is outputted and the second time the VCO frequency is outputted respectively, the corresponding control voltage signals (outputted from the loop filter and inherently detected by the VCO) and the corresponding division values (N1 and N2); and, substituting for fo the frequency gain of the VCO is calculated by Fin (NI-N2)/ (V1-V2) or in order to monitor the performance of the VCO or the PLL. Therefore, it would have been obvious to one of ordinary skill in the art to measure the frequency gain of the VCO for the reason stated above.

As to claim 10, Owen discloses a PLL circuit comprising: a phase detector (Fig. 3, block 7) for comparing phases of first and second signals applied thereto with each other and outputting a phase error signal when there is a phase difference between the first and second signals; a loop filter (block 9) for filtering the phase error signal

outputted from the phase detector, stabilizing the filtered phase error signal, and outputting a control signal; a voltage controlled oscillator (block 1) for controlling frequency gain (e.g. tuning sensitivity) of a signal output in response to the control signal outputted from the loop filter (Col. 1, lines 51-61); and a divider (block 6; Col. 2, lines 35-49) for dividing the frequency of the outputted signal of the voltage controlled oscillator according to a division rate to apply the outputted signal to the phase detector as the second signal, wherein the frequency gain (e.g. rate of change of Kv or Kvco) is represented as the slope or rate of change of the VCO gain (Fig. 1a; Col. 2, lines 19-22). Owen is not explicit about calculating the frequency gain of the VCO as Fstep/ (V1-V2). One of ordinary skill in the art would recognize that the VCO gain (e.g. Kv or Kvco) is a well know parameter that is related to the output signal of the VCO (fo(t)) divided by the input signal of the VCO (V(t)). Therefore, one of ordinary skill in the art would recognize that the rate of change or slope of the VCO gain is calculated as [(fo1-fo2) = Fstep]/ (V1-V2), wherein indices 1 and 2 corresponds to the first time that the VCO frequency (fo) is outputted and the second time the VCO frequency is outputted respectively, the corresponding control voltage signals (outputted from the loop filter and inherently detected by the VCO) and the corresponding division values (N1 and N2) in order to monitor the performance of the VCO or the PLL. Therefore, it would have been obvious to one of ordinary skill in the art to measure the frequency gain of the VCO for the reason stated above.

As to claim 12, Owen discloses a PLL circuit comprising: a phase detector (Fig. 3, block 7) for comparing phases of first and second signals applied thereto with each

other and outputting a phase error signal when there is a phase difference between the first and second signals; a loop filter (block 9) for filtering the phase error signal outputted from the phase detector, stabilizing the filtered phase error signal, and outputting a control signal; a voltage controlled oscillator (block 1) for controlling frequency gain (e.g. tuning sensitivity) of a signal output in response to the control signal outputted from the loop filter (Col. 1, lines 51-61); and a divider (block 6; Col. 2, lines 35-49) for dividing the frequency of the outputted signal of the voltage controlled oscillator according to a division rate to apply the outputted signal to the phase detector as the second signal, wherein the frequency gain (e.g. rate of change of Kv or Kvco) is represented as the slope or rate of change of the VCO gain (Fig. 1a; Col. 2, lines 19-22). Owen is not explicit about calculating the frequency gain of the VCO as (F1-F2)/(V1-V2). One of ordinary skill in the art would recognize that the VCO gain (e.g. Kv or Kvco) is a well know parameter that is related to the output signal of the VCO (fo(t)) divided by the input signal of the VCO (V(t)). Also, the relationship between the reference frequency (e.g. Fin as named by the applicant in this claim) and the output frequency of the VCO is fo = N * Fin. Consequently, one of ordinary skill in the art would recognize that the rate of change or slope of the VCO gain is calculated as (fo1-fo2)/(V1-V2), wherein indicies 1 and 2 corresponds to the first time that the VCO frequency (fo) is outputted (e.g. F1) and the second time the VCO frequency is outputted (e.g. F2) respectively, the corresponding control voltage signals (outputted from the loop filter and inherently detected by the VCO) and the corresponding division values (N1 and N2) in order to monitor the performance of the VCO or the PLL device. Therefore, it would

have been obvious to one of ordinary skill in the art to measure the frequency gain of the VCO for the reason stated above.

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Owen et al, and further in view of Davis et al.

As to claim 14, Owen discloses a PLL circuit comprising: a phase detector (Fig. 3, block 7) for comparing phases of first and second signals applied thereto with each other and outputting a phase error signal when there is a phase difference between the first and second signals; a loop filter (block 9) for filtering the phase error signal outputted from the phase detector, stabilizing the filtered phase error signal, and outputting a control signal; a voltage controlled oscillator (block 1) for controlling frequency gain (e.g. tuning sensitivity) of a signal output in response to the control signal outputted from the loop filter (Col. 1, lines 51-61); and a divider (block 6; Col. 2, lines 35-49) for dividing the frequency of the outputted signal of the voltage controlled oscillator according to a division rate to apply the outputted signal to the phase detector as the second signal and repeating the above steps till the lock condition is reached, wherein the frequency gain (e.g. rate of change of Kv or Kvco) is represented as the slope or rate of change of the VCO gain (Fig. 1a; Col. 2, lines 19-22). Owen is not explicit about calculating the frequency gain of the VCO as Fin (NI-N2)/ (V1-V2); and also, controlling gains of the phase detector and loop filter by adjusting the variable current source of the charge pump circuit. One of ordinary skill in the art would recognize that the VCO gain (e.g. Kv or Kvco) is a well know parameter that is related to

the output signal of the VCO (fo(t)) divided by the input signal of the VCO (V(t)). Therefore, one of ordinary skill in the art would recognize that the rate of change or slope of the VCO gain is calculated as [(fo1-fo2) = Fstep]/ (V1-V2), wherein indicies 1 and 2 corresponds to the first time that the VCO frequency (fo) is outputted and the second time the VCO frequency is outputted respectively, the corresponding control voltage signals (outputted from the loop filter and inherently detected by the VCO) and the corresponding division values (N1 and N2) in order to monitor the performance of the VCO or the PLL. Therefore, it would have been obvious to one of ordinary skill in the art to measure the frequency gain of the VCO for the reason stated above. Davis discloses a PLL comprising a phase detector that includes a charge pump, wherein the phase gain of the phase detector is controlled by adjusting a current source included in the charge pump circuit in order to ensure that the operational characteristics of the current generators are in agreement prior to the start of each phase correction thus preventing steady-state phase alignment errors from developing between the reference and recovered signals (Fig. 2, block 68; Col. 3, lines 40-48; Col. 4, lines 5-13). Therefore, it would have been obvious to one of ordinary skill in the art to incorporate adjusting the current source of the charge pump by Davis into the invention of Owen for the reason stated above.

Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Owen et al, and further in view of Walley.

As to claim 16, Owen discloses a PLL circuit comprising: a phase detector (Fig. 3, block 7) for comparing phases of first and second signals applied thereto with each

other and outputting a phase error signal when there is a phase difference between the first and second signals; a loop filter (block 9) for filtering the phase error signal outputted from the phase detector, stabilizing the filtered phase error signal, and outputting a control signal; a voltage controlled oscillator (block 1) for controlling frequency gain (e.g. tuning sensitivity) of a signal output in response to the control signal outputted from the loop filter (Col. 1, lines 51-61); and a divider (block 6; Col. 2, lines 35-49) for dividing the frequency of the outputted signal of the voltage controlled oscillator according to a division rate to apply the outputted signal to the phase detector as the second signal, wherein the frequency gain (e.g. rate of change of Kv or Kvco) is represented as the slope or rate of change of the VCO gain (Fig. 1a; Col. 2, lines 19-22). Owen is not explicit about calculating the frequency gain of the VCO as (F1-F2)/(V1-V2); and also, the gain of the phase detector or gain of the loop filter to control the loop gain. One of ordinary skill in the art would recognize that the VCO gain (e.g. Kv or Kvco) is a well know parameter that is related to the output signal of the VCO (fo(t)) divided by the input signal of the VCO (V(t)). Also, the relationship between the reference frequency (e.g. Fin as named by the applicant in this claim) and the output frequency of the VCO is fo = N * Fin. Consequently, one of ordinary skill in the art would recognize that the rate of change or slope of the VCO gain is calculated as (fo1-fo2)/(V1-V2), wherein indices 1 and 2 corresponds to the first time that the VCO frequency (fo) is outputted (e.g. F1) and the second time the VCO frequency is outputted (e.g. F2) respectively, the corresponding control voltage signals (outputted from the loop filter and inherently detected by the VCO) and the corresponding division values (N1 and N2)

in order to monitor the performance of the VCO or the PLL device. Therefore, it would have been obvious to one of ordinary skill in the art to measure the frequency gain of the VCO for the reason stated above. Walley discloses a PLL comprising a phase detector that includes a charge pump (optional), wherein the phase gain of the adjusted according to a control signal outputted from a controller in order to control the loop gain to be uniform (Fig. 3, blocks 313, 325, and 327). Therefore, it would have been obvious to one of ordinary skill in the art to incorporate controlling the gain loop be adjusting the gain of the phase comparator or gain of the loop filter as taught by Walley into the invention of Owen for the reason stated above.

Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Owen et al, and further in view of Kobayashi et al (US 2002/0005764).

As to claim 18, Owen discloses a PLL circuit comprising: a phase detector (Fig. 3, block 7) for comparing phases of first and second signals applied thereto with each other and outputting a phase error signal when there is a phase difference between the first and second signals; a loop filter (block 9) for filtering the phase error signal outputted from the phase detector, stabilizing the filtered phase error signal, and outputting a control signal; a voltage controlled oscillator (block 1) for controlling frequency gain (e.g. tuning sensitivity) of a signal output in response to the control signal outputted from the loop filter (Col. 1, lines 51-61); and a divider (block 6; Col. 2, lines 35-49) for dividing the frequency of the outputted signal of the voltage controlled oscillator according to a division rate to apply the outputted signal to the phase detector

as the second signal, wherein the frequency gain (e.g. rate of change of Kv or Kvco) is represented as the slope or rate of change of the VCO gain (Fig. 1a; Col. 2, lines 19-22). Owen is not explicit about calculating the frequency gain of the VCO as (F1-F2)/(V1-V2); and also, comparing the calculated frequency gain with a predetermined reference gain and controlling the frequency gain of the voltage controlled oscillator to be uniform. One of ordinary skill in the art would recognize that the VCO gain (e.g. Kv or Kvco) is a well know parameter that is related to the output signal of the VCO (fo(t)) divided by the input signal of the VCO (V(t)). Also, the relationship between the reference frequency (e.g. Fin as named by the applicant in this claim) and the output frequency of the VCO is fo = N * Fin. Consequently, one of ordinary skill in the art would recognize that the rate of change or slope of the VCO gain is calculated as (fo1-fo2)/(V1-V2), wherein indicies 1 and 2 corresponds to the first time that the VCO frequency (fo) is outputted (e.g. F1) and the second time the VCO frequency is outputted (e.g. F2) respectively, the corresponding control voltage signals (outputted from the loop filter) and the corresponding division values (N1 and N2) in order to monitor the performance of the VCO or the PLL device. Therefore, it would have been obvious to one of ordinary skill in the art to measure the frequency gain of the VCO for the reason stated above. One of ordinary skill in the art would recognize that monitoring the frequency gain of the VCO with respect to different parameters such as a predetermined reference gain could be performed as it is evidenced by Kobayashi (Fig. 2 and 3) in order to obtain more information than only the frequency gain of the VCO. Therefore, it would have been obvious to one of ordinary skill in the art to monitoring the frequency gain of the VCO

with respect to different parameters such as a predetermined reference gain for the reason stated above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Freshteh N. Aghdam whose telephone number is 571-272-6037. The examiner can normally be reached on 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on 571-272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Freshteh N. Aghdam
Examiner
Art Unit 2611

January 10, 2008

CHIEH M. FAN
SUPERVISORY PATENT EXAMINER